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<u>Amendments to the Claims:</u>

The following claims will replace all prior versions of the claims in this application (in the unlikely event that no claims follow herein, the previously pending claims will remain):

1. (Currently Amended) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant over on a semiconductor substrate which has gone through predetermined processes;

forming sequentially a first metal layer and a poly-silicon layer over on the dielectric layer;

forming a poly-silicon layer on the first metal layer;

forming an upper electrode pattern by patterning the poly-silicon layer and the first metal layer;

forming a second metal layer covering the upper electrode pattern on patterned poly-silicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer; and

forming an upper electrode constituted with the second metal layer, the poly-silicon layer and the first metal layer by patterning the second metal layer so that the second metal layer is connected to the first metal layer to thereby form an upper electrode constituted with the patterned second metal layer, the patterned poly-silicon layer, and the patterned first metal layer.

- 2. (Original) The method as recited in claim 1, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.
- 3. (Original) The method as recited in claim 2, wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process.
- 4. (Original) The method as recited in claim 3, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.
- 5. (Previously Presented) The method as recited in claim 1, wherein the second metal layer is constituted with one of a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.